THE DIFFERENTIAL REFERENCE FREQUENCY SYNTHESIZER

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ABSTRACT

Indirect digital frequency synthesizers cannot achieve fast frequency switching with closely spaced frequencies because of limitations imposed by the requisite narrow loop bandwidth. A novel dual-loop digital frequency synthesizer is presented which satisfies these conflicting requirements and, in most cases, exhibits improved phase noise performance.

INTRODUCTION

Dual-loop digital frequency synthesizers have been used in many applications and are covered extensively in the literature (1,2, 3,4). An example of such a synthesizer is shown in Figure 1 and consists of two interconnected digital phase-lock loops (PLLs) such that PLL1 serves as a frequency agile offset generator for PLL2. In this example the PLL1 voltage-controlled oscillator (VCO) output frequency is downconverted, with the aid of an offset frequency F_O, to a suitably selected lower frequency F_{D1} serving as the input frequency of the digital divider. The reference F_{R1} and the divider output signals are applied to the inputs of the phase/frequency detector, the output of which is amplified, filtered and fed to the tuning port of VCO1. A variable gain loop amplifier is needed to compensate for variations in loop gain as a function of the division ratio. Consequently, a design with a minimum range of division ratios is advantageous. If used, F_O must either be below the lowest or above the highest output frequency F(M). PLL2 is similar to PLL1 except for its reference frequency F_{R2} and its agile offset frequency F(M). Its output frequency F(M,N) is given by

$$F(M,N) = F_O + MF_{R1} + NF_{R2} \text{ for } F_O < F(M) < F(M,N) \qquad (1)$$

and its output frequency spacing F_S is equal to F_{R1}. For example, to synthesize 100 frequencies with a frequency spacing of F_S, F_{R1} and F_{R2} could be F_S and $10F_S$, respectively, and the lowest division ratios (M and N) would be one through ten. Frequency switching is then performed by programming suitable frequency division ratios M and N via the frequency select command.

Frequency switching time (including frequency settling time) exhibits an inverse dependence on loop bandwidth which must be substantially smaller than the reference frequency (typically 10 percent) in order to provide adequate attenuation to the reference signal. Therefore, synthesis of closely spaced frequencies requires that one of the PLLs (PLL1 in the example) has a narrow bandwidth, resulting in a long frequency switching time. In addition, the open-loop gain of narrowband PLLs is limited by stability considerations and prevents the VCO phase noise (inside the loop bandwidth) from being degenerated to the noise floor of the loop.

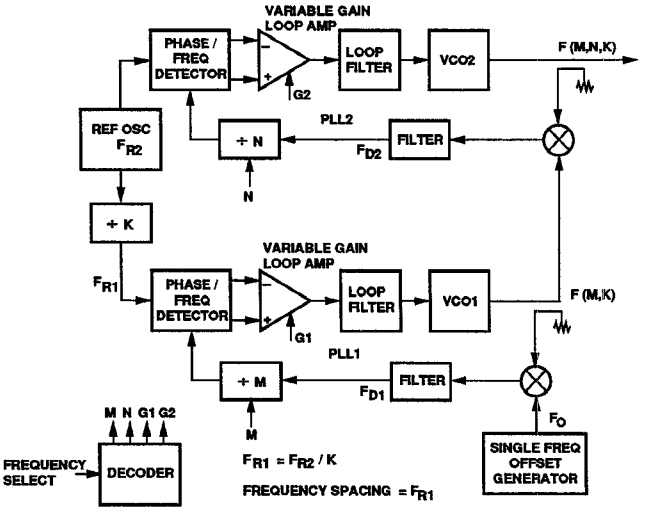

FIGURE 1. CONVENTIONAL DUAL-LOOP FREQUENCY SYNTHESIZER

The conflicting requirements of synthesizing closely spaced frequencies with fast frequency switching can be satisfied using a novel dual-loop digital synthesizer called the Differential Reference Frequency Synthesizer (DRFS) (5). Fast frequency switching is possible because the DRFS design is based on wideband PLLs. In addition, wider loop bandwidths allows higher open-loop gains which result in reduced phase noise.

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A block diagram of the DRFS is shown in Figure 2. Although it is similar to the one shown in Figure 1, its uniqueness and novelty are that it can synthesize closely spaced frequencies with two PLLs having reference frequencies F_{R1} and F_{R2} that are larger than the output frequency spacing F_S. The only conditions are that the difference between F_{R1} and F_{R2} must be equal to F_S and that each one must be an integer multiple of F_S, thereby making them synchronous. PLL1 may have a fixed offset frequency F_O and its output frequency F(M) serves as the frequency agile offset signal for PLL2. The PLL2 output frequency F(M,N) is given by the expression in (1).

The lowest M and N values needed to synthesize the 100 frequencies of the previous example were computed for the general case of $F_O = 0$ and an arbitrarily selected reference pair of $6F_S$ and $7F_S$, and are listed in the matrix in Figure 3. In this case the division ratios do not vary consecutively with the synthesized frequencies. Also, from Figure 3 it is evident that, with the selected offset

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frequency, not all of the lowest 42 (M times N) frequencies can be synthesized. To synthesize all the frequencies (with a slight increase in the maximum frequency division ratio), the offset frequency can be moved to $43F_S$ below the lowest output frequency.

Although the range of frequency division ratios in Figure 3 (14:1) is greater than in the previous example (10:1), the DRFS offers the capability to synthesize closely spaced frequencies with fast frequency switching.

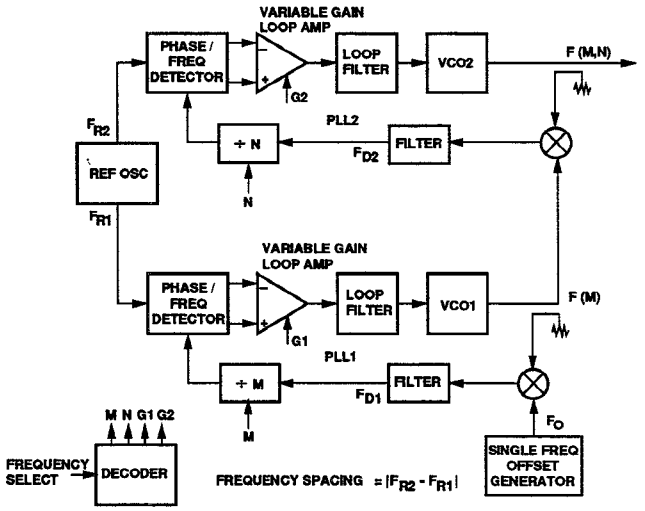

FIGURE 2. DIFFERENTIAL REFERENCE FREQUENCY SYNTHESIZER (DRFS)

M, N VALUES FOR NORMALIZED REFERENCE FREQUENCIES 6, 7

	0	1	2	3	4	5	6	7	8	9
0	****	****	****	****	****	****	****	****	****	****
1	****	****	****	1, 1	****	****	****	****	****	2, 1
2	1, 2	****	****	****	****	3, 1	2, 2	1, 3	****	****
3	****	4, 1	3, 2	2, 3	1, 4	****	****	5, 1	4, 2	3, 3
4	2, 4	1, 5	****	6, 1	5, 2	4, 3	3, 4	2, 5	1, 6	7, 1
5	6, 2	5, 3	4, 4	3, 5	2, 6	1, 7	7, 2	6, 3	5, 4	4, 5
6	3, 6	2, 7	8, 2	7, 3	6, 4	5, 5	4, 6	3, 7	2, 8	8, 3
7	7, 4	6, 5	5, 6	4, 7	3, 8	9, 3	8, 4	7, 5	6, 6	5, 7
8	4, 8	3, 9	9, 4	8, 5	7, 6	6, 7	5, 8	4, 9	10, 4	9, 5
9	8, 6	7, 7	6, 8	5, 9	4,10	10, 5	9, 6	8, 7	7, 8	6, 9
10	5,10	11, 5	10, 6	9, 7	8, 8	7, 9	6,10	5,11	11, 6	10, 7
11	9, 8	8, 9	7,10	6,11	12, 6	11, 7	10, 8	9, 9	8,10	7,11
12	6,12	12, 7	11, 8	10, 9	9,10	8,11	7,12	13, 7	12, 8	11, 9
13	10,10	9,11	8,12	7,13	13, 8	12, 9	11,10	10,11	9,12	8,13
14	14, 8	13, 9	12,10							

HIGHEST FREQUENCY DIVISION RATIO: 14

FIGURE 3. MATRIX OF FREQUENCY DIVISION RATIOS FOR THE DRFS

$F_{R1} / F_S = 6$

$F_{R2} / F_S = 7$

F_S = FREQUENCY SPACING

MODIFIED DIFFERENTIAL REFERENCE FREQUENCY SYNTHESIZER (MDRFS)

The frequency division ratio ranges of the DRFS can be reduced using the MDRFS, shown in the block diagram of Figure 4. The main difference between the MDRFS and the DRFS is in the offset frequencies of the two PLLs which are based on the "Center Offset" concept (6). In PLL1 the offset frequency is placed either at, or close to, the center of the PLL1 output frequency range. This creates an ambiguity because every downconverted frequency F_{D1} has two corresponding VCO frequencies. This ambiguity is eliminated by the VCO coarse-tuning circuit which, following the frequency select command, positions the VCO frequency at some arbitrary frequency on the correct side of the offset frequency. Because an opposite relationship exists between F_{D1} and its two corresponding VCO frequencies, the loop is unstable for all VCO frequencies on one side of the offset frequency. This instability is eliminated by interchanging the two outputs of the phase/frequency detector with the transfer switch SW1. The output frequency F(M) of PLL1 is expressed as

$$F(M) = F_O \pm MF_{R1} \quad M = 1,2,3... \tag{2}$$

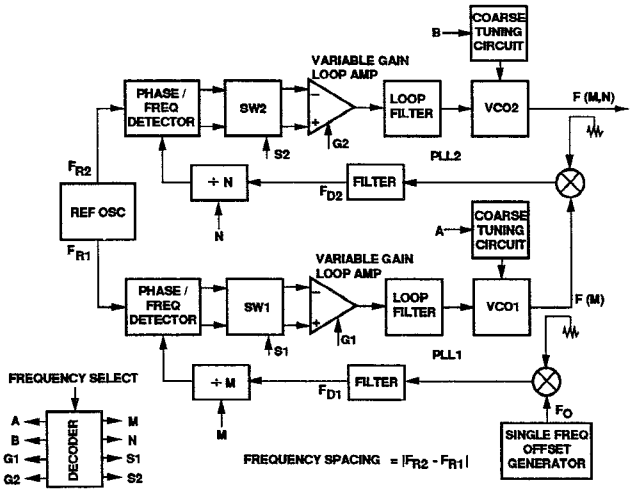

FIGURE 4. MODIFIED DIFFERENTIAL REFERENCE FREQUENCY SYNTHESIZER (MDRFS)

The output of PLL1 serves as the agile offset frequency for PLL2, and PLL2 exhibits the same dual relationship between F_{D2} and the VCO frequencies. The MDRFS output frequency F(M,N) is given by the expression

$$F(M,N) = F_O \pm MF_{R1} \pm NF_{R2} \tag{3}$$

The matrix in Figure 5 presents the lowest M,N pairs needed to synthesize the 100 frequencies of the previous example, using the previously selected reference frequencies. The negative matrix indices indicate synthesizer output frequencies which are below F_O and the negative division ratios indicate PLL output frequencies which are below the respective PLL offset frequencies. As can be seen, the range of frequency division ratios has been reduced from 14:1 in the DRFS to 12:1 in the MDRFS. This reduction is even more pronounced for a larger number of output frequencies.

M, N VALUES FOR NORMALIZED REFERENCE FREQUENCIES 6, 7

	0	1	2	3	4	5	6	7	8	9
-4	-2, -4	-1, -5	7, -12	-6, -1	-5, -2	-4, -3	-3, -4	-2, -5	-1, -6	-7, -1
-3	2, -6	-4, -1	-3, -2	-2, -3	-1, -4	-7, 1	1, -6	-5, -1	-4, -2	-3, -3
-2	-1, -2	-7, 3	1, -4	-5, 1	3, -6	-3, -1	-2, -2	-1, -3	-7, 2	1, -5
-1	-4, 2	-3, 1	5, -6	-1, -1	-7, 4	1, -3	2, -4	-4, 1	4, -6	-2, -1
0	-7, 6	1, -1	2, -2	3, -3	-3, 2	-2, 1	6, -6	-7, 5	1, -2	2, -3
0	7, -6	-1, 1	-2, 2	-3, 3	3, -2	2, -1	-6, 6	7, -5	-1, 2	-2, 3
1	4, -2	3, -1	-5, 6	1, 1	7, -4	-1, 3	-2, 4	4, -1	-4, 6	2, 1
2	1, 2	7, -3	-1, 4	5, -1	-3, 6	3, 1	2, 2	1, 3	7, -2	-1, 5
3	-2, 6	4, 1	3, 2	2, 3	1, 4	7, -1	-1, 6	5, 1	4, 2	3, 3
4	2, 4	1, 5	-7, 12	6, 1	5, 2	4, 3	3, 4	2, 5	1, 6	7, 1
5	6, 2									

HIGHEST FREQUENCY DIVISION RATIO: 12

FIGURE 5. MATRIX OF FREQUENCY DIVISION RATIOS FOR THE MDRFS

$F_{R1} / F_S = 6$

$F_{R2} / F_S = 7$

F_S = FREQUENCY SPACING

SUMMARY

Two realizations of the novel DRFS were presented (although more possibilities exist) and compared to a conventional dual-loop digital synthesizer using an example. From this example it is evident that use of the DRFS allows synthesis of closely spaced frequencies with PLLs that use arbitrarily high reference frequencies and, therefore, can have considerably wider bandwidths and commensurately shorter frequency switching times than is possible to achieve with conventional dual-loop synthesizers. Furthermore, a wider loop bandwidth allows the realization of a higher open-loop gain which, in many applications, results in improved phase noise performance.

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